

Status of LC R&D Proposals at Oklahoma

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OUTLINE

- LC R&D Interests
- CCD Tests
- Software Tools



Possible Vertex Detector Options

- CCD:
 - Thickness of the sensitive region $\sim 20 \mu\text{m}$
 - Wafer thickness can be thinned down to $\sim 20\mu\text{m}$
 - Relatively sensitive to radiation damage
- CMOS pixel sensor:
 - Sensor diode and read-out amplifier
 - Signals from pixels are read out by X-Y addressing
 - Thickness of the sensitive region $\sim 20\mu\text{m}$
 - Radiation immunity is better than that of CCDs
- Hybrid pixel sensor:
 - Sensor diode wafer and readout wafer connected by bump bonding technique
 - Thicker than CCDs or CMOS sensors
 - Radiation hardness is excellent



LC Software Interest (DOE)

- Monte Carlo studies of Silicon Tracker and/or CCD Detector
 - » Optimize design, including number of layers, forward region (pixels?)
 - » Test and develop pattern recognition. How many layers are necessary?
- Past Experience (Mike Strauss)
 - » Developed clustering algorithms, and track finding for SLD VXD2, and optimization of VXD3 design.
 - » Developed Monte Carlo simulation of VXD2 and VXD3 including charge deposition and integration.
 - » Developed pattern recognition and track finding for TPC at PEP.



LC Hardware Interest (NSF)

➤ CCD Research and Development

- » Test properties of CCDs
 - > Help answer questions about use of CCDs in LC environment.
- » Develop new CCD support technology, particularly electronic connections and components
- » Thinning and radiation tests, establish relationships with vendors
- » Readout design, DAQ (UCLC proposal)

➤ Past Experience

- » Tested microstrip detectors now installed in DO, CLEO III
- » Developed flex connectors for CLEO III
- » Developing and testing flex circuits for ATLAS Pixel detector
- » Contributed to ATLAS pixel readout design



NSF Proposal

- UCLC proposal: “Development and design of an LC ASIC for CCD readout and data reduction”
 - » Three year project
 - » Collaboration between OU, Boston U. (Ulrich Heintz), and Fermilab (William Wester)
 - » Previous experience on ATLAS pixel detector which uses IBM deep-submicron process



Personnel

- **OUHEP**
 - » Electronics Engineer (Base program)
 - » EE Master's student (ASIC design)
 - » Test facilities
- **BU**
 - » ASIC designer
 - » Graduate student
 - » Test facilities
- **Fermilab (Base program)**
 - » ASIC design group
 - » Test facilities
 - » Silicon lab



CCD Requirements (Nikolai Sinev)

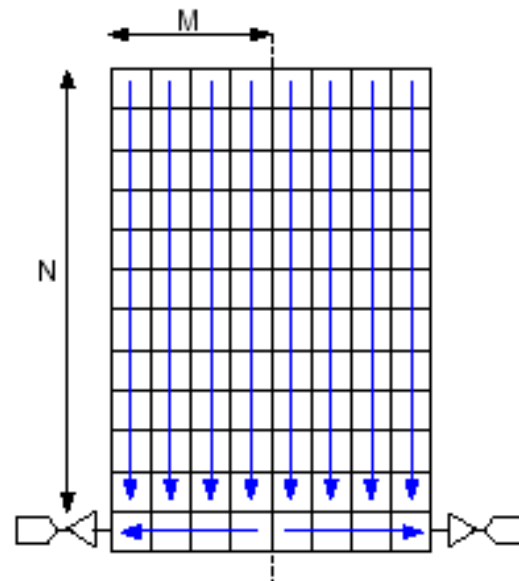
Readout speed challenge

- Requirement for NLC/JLC **~8 msec** readout time
- Requirement for TESLA **~50 μ sec** (due to large number of bunches in a pulse train)
- VXD3 readout time is **200 msec** with **5 MHz** clock speed and 4 output nodes/CCD. Clock speed **10 MHz** was tested – no problems. **50 MHz** clock speed was tested by UK group. It works. Remaining factor of 2.5 in reduction of readout time can be achieved by increasing number of outputs. **12 - 16** outputs/CCD will do the trick for NLC/JLC.
- Task for the TESLA is more challenging, but also feasible. UK group has reported arrival of first prototype CCD with *column parallel readout*. Essentially this is equivalent to increasing number of outputs per CCD to hundreds or even thousands. There are electronics challenges on this way, mainly related to power dissipation on CCD. However, taking into account duty factor of about 200 for TESLA, pulsed power may solve such problems.

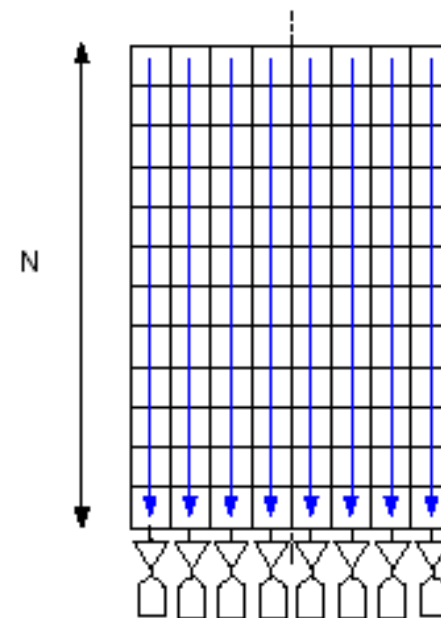


Column Parallel CCD (Konstantin Stefanov)

- Serial register is omitted
- Maximum possible speed from a CCD (tens of Gpix/s)
- Image section (high capacitance) is clocked at high frequency
- Each column has its own amplifier and ADC – requires readout chip



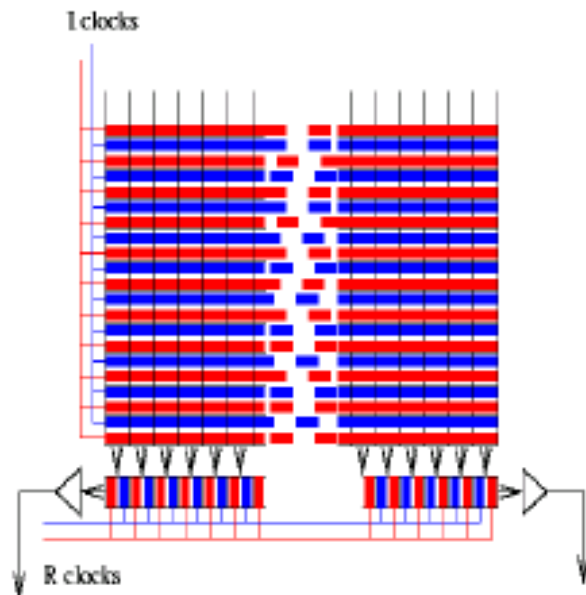
“Classic CCD”
Readout time $\approx N \times M / F_{out}$



Column Parallel CCD
Readout time $= N / F_{out}$

CCD Readout Challenge (Nikolai Sinev)

Readout speed challenge – more



$$T_{read} = N_{rows} * (T_i + N_{col} * T_r)$$

For VXD3 $T_i=20 \mu\text{sec}$ $T_r=200 \text{ nsec}$

$N_{rows} = 2000$, $N_{col}=400$, $N_{pix}=8 \times 10^5$

(per node, per CCD $N_{pix}=3.2 \times 10^6$)

For TESLA assume N_{pix} same, $T_r=0$

Because of absence of R register,

$N_{rows} = N_{pix}/N_{nodes} \sim 1000$.

To get $T_{read}=50 \mu\text{sec}$ T_i should be 50 nsec ,

meaning I clock frequency 20 MHz

But capacitance of I clock bus is 40 nF

instead of $< 100 \text{ pF}$ for R clock bus.

Its impedance for 20 MHz is 0.2Ω ,

which leads to I clock current $\sim 50 \text{ A/CCD}$ (with

10 V clocks).

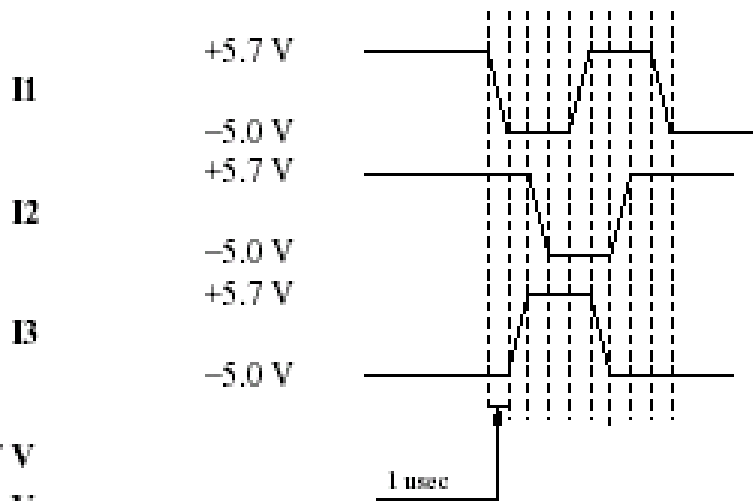
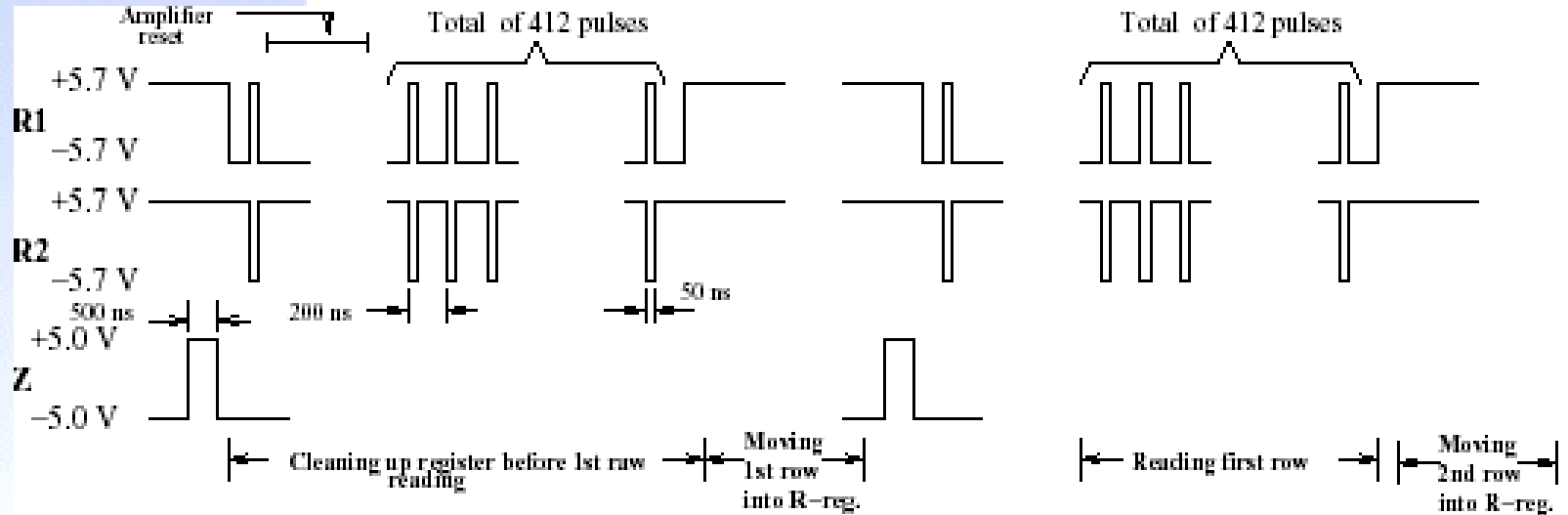
Tests at OU with VXD3 CCD Started (with help from Jim Brau and Nick Sinev)



Test Setup



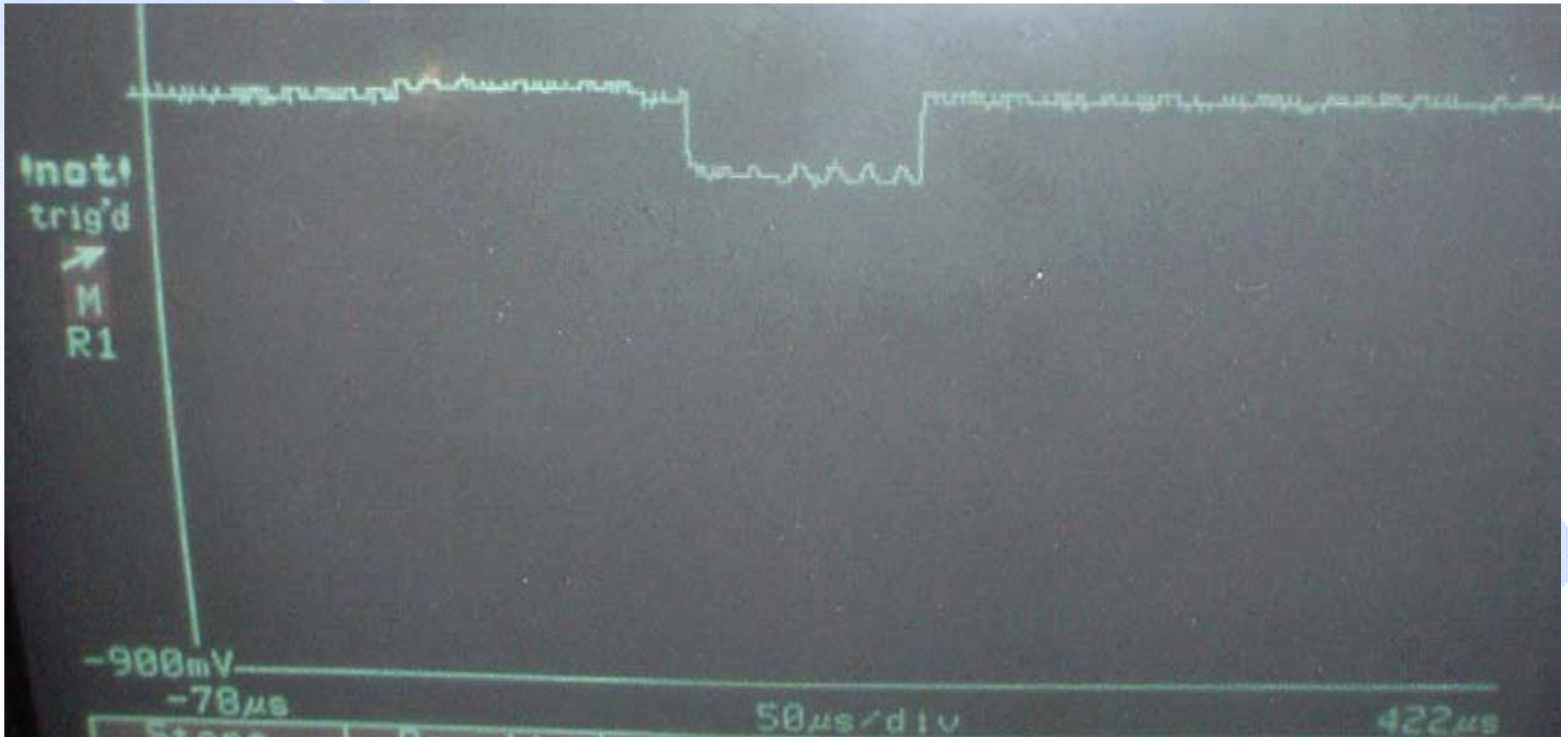
Clock Timing



VDD = + 17 V
 VRD = + 13 V
 VOG = - 2 V



Readout of Two Rows (Room Temperature)



CCD Test Goals

- Gain First Experience with CCD readout
 - » Source Response
 - » Laser Response
- Study Clock Timing
 - » Readout Speed
 - » Temperature Dependence

Software: Cadence Tools at OU

- **Virtuoso Custom Designer**
- **Assura Physical Verification Tools**
- **Ambit Build Gates**
- **Allegro**
- **Silicon Ensemble**
- **Spectre Simulator**
- **Verilog-XL**

Process Design Kits Installed

- TSMC 0.25 Micron
- TSMC 0.35 Micron
- TSMC 0.18 Micron
- HP 0.5 Micron
- AMI 0.6 Micron
- AMI 1.6 Micron



Conclusions

- CCD Tests at OU have been Started
- Software Tools for VLSI Design are Installed and Tested
- Contacts with Others Interested in Vertex Detector Readout have been made
 - » Oregon/Yale group
 - » LCFI group
 - » SLAC
 - » Fermilab

